Low Voltage Micro-Phasor Measurement Unit (μPMU)

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Abstract—**Phasor measurement units (PMUs) installed in the power grid are currently positioned mainly on the transmission system or in substations. A PMU creating real-time synchrophasor data from the consumer voltage level, called μPMUs, could provide new insight into modern power systems. These units can be created more cheaply, an order of magnitude less, than current commercial PMUs. For this reason, many more PMUs could be deployed and provide a much higher resolution of the distribution grid. There are many new applications for such a visible grid in post-mortem event analysis and identification, as well as near real-time monitoring. This paper describes the hardware limitations impact on developing an accurate synchrophasor along with considerations for μPMUs placement within the distribution grid.**

Index Terms—**Phasor Measurement Unit, Synchrophasor, Micro-PMU, μPMU**

I. INTRODUCTION

THE μPMU built by our group is intended to serve as a means of understanding how PMUs are built and operated due to a majority of them not completely complying with existing IEEE synchrophasor standards. In order to understand these proprietary commercial units, an open-box μPMU, shown in Fig. 1 and Fig. 2, was developed and deployed. Figure 3 shows the overview of the device set-up.

The main function of the device is to calculate voltage, frequency, and phase at the household voltage level. A GPS is used for time-stamping the data in order to have the same time reference across all PMUs, according to the IEEE c37.118 standards. Data is then sent to an openPDC server to be displayed and archived. Archived data can be used for system model validation as well as identifying causes of grid instabilities.

Key μPMU features include high sampling frequency of 10 kS/s, user selectable phasor output rate, LCD to show live data to user, and battery backup supply to allow continuous operations up to one hour during grid instabilities. Furthermore, the cost of producing a unit is only around $350, making it much cheaper than other PMUs, and thus more units could be deployed.

II. HARDWARE ISSUES

A. Description of Software Operation

In order to explore issues due to hardware specifications, one must briefly understand how the program derives synchrophasors. While the end result is the same, PMUs produced by different companies can have very different software implementations.

In our case, the μPMU collects 10 kS/s. Once a second passes, indicated by the GPS second pulse, data collected during the previous second is divided into fragments, each with the same amount of data points, according to the selected output rate. For a 10 Hz output rate, each fragment would consist of 1000 samples because of the 10 kS/s sampling frequency. The program then calculates the RMS voltage, frequency, phase and assigns a timestamp to each fragment before uploading it to the openPDC server, where data is displayed
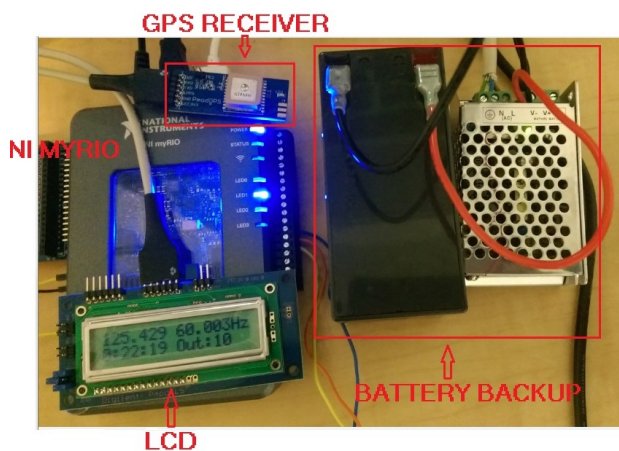

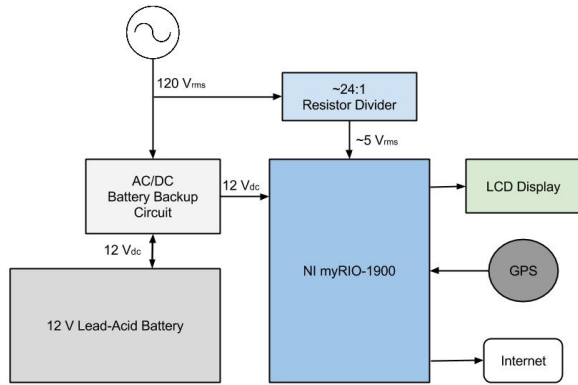Fig. 1. μPMU components

Fig. 2. μPMU operating in housing

Fig. 3. μPMU diagram

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and archived. Each fragment is called a synchrophasor. The reason for not processing the data points as they become available, but rather waiting for a second worth of data is discussed in section C.

B. Effects of Hardware Limitations on Synchrophasors

The μPMU is designed using National Instruments myRIO-1900 and LabVIEW software. The myRIO has a 40 MHz clock, which directly impacts synchrophasors depending on what the user selects as the output rate. The output rates considered are 10, 20, 30, 40, and 60 Hz. Sampling frequency of 10 kS/s allows data points to be evenly spaced for a 10, 20, and 40 Hz output rate. However, the sampling frequency does not evenly divide by the 30 and 60 Hz output rates, in which case a different sampling frequency must be chosen. Moreover, this new frequency must be divisible by 60 while the 40 MHz clock needs to be divisible by the frequency in order to ensure exact timing between samples. This is a problem because no sampling frequency can satisfy both criteria. The frequency with the least error is 5940 S/s; but each sample will be spaced by 40 MHz / 5940 = 6734.01 clock ticks. The software can not operate with fraction of ticks, therefore it will round the spacing between samples to 6734 ticks. This rounding introduces a timing error of 1 μs after the first 4000 samples, with the timing error growing with each sample taken. Unless a hardware with an appropriate clock speed is used, an output rate of 30 or 60 Hz will have inherent timing errors, which come before even considering other sources of error that are discussed next.

The myRIOs 40 MHz clock has significant drift that was previously neglected. It was later measured that the clock varies by the manufacturer specified maximum drift of 1 μs/s. This is in addition to the maximum allowed 1 μs GPS clock error which is inherent to the GPS systems design and operation. This FPGA clock error has an undesired and very influential effect on the synchrophasor measurements and will be further discussed with respect to calculating frequency,

voltage, phase, and timestamp. The theoretical effects of a 40 ticks clock error, corresponding to 1 μs, will be explored.

When it comes to calculating frequency, a 40 ticks clock deficit will translate to a 60 μHz error during each second and divide itself evenly to each synchrophasor, the number of synchrophasors depending on the output rate. The error will not propagate to the next synchrophasor as each has its frequency calculated independently and is considered to be within the allowed limits; according to the IEEE synchrophasor standards, source [8], the maximum allowed frequency error is 0.005 Hz.

Phase calculation error has the potential to be propagated through from second to second if code is not implemented to take care of the FPGA clock error as described in part C, and phase error will reach the 26 μs allowed error limit in 26 seconds. The FPGA clock error fix will limit the phase error to 1 μs, which corresponds to 0.022 degrees for a 60 Hz system.

Calculating RMS voltage only depends on data values as long as they are evenly spaced on the time axis; it is assumed that the FPGA clock remains relatively constant during 1 second, only changing over long periods of time. Therefore, calculated RMS voltage is considered to be error free when considering the effect of clock error.

According to [8], timestamp is defined as the time in the middle of the synchrophasor. Timestamp error depends on the output rate. In the case of a 10 Hz rate, the error in timestamp due to a 1 μs clock error is 0.05 μs for the first synchrophasor in the second. This error adds up, with the last synchrophasor in the second having a timestamp error of 0.95 μs. This is in addition to the maximum 1 μs error inherent to the GPS system. Due to the FPGA clock error fix, the error is cleared after each second; therefore, the maximum timestamp error will be 1.95 μs for a 10 Hz output rate.

C. FPGA Clock Drift

In order to stop the propagation of error in phase and timestamp calculation from second to second, the program had to be changed such that it fixes the FPGA clock error. This ideas is described next: theoretically, with a perfect FPGA clock, the device samples the voltage at 10 kS/s and each synchrophasor would consist of calculations made on 1000 data points in the case of a 10 Hz output rate. Instead, knowing the clock is not exactly 40 MHz, the program is set up in a way that it allows it to measure exactly how many samples have been taken during the last second, which might not have been 10,000. The downside is the 1 second latency between the time when data was taken and when the synchrophasor is ready to be sent to the user, which might play a role if real time data is needed.

III. MEASUREMENT LOCATION

The μPMUs are to be placed in selected locations such that synchrophasors will provide a meaningful interpretation of the distribution grid. There are many factors which drive the optimum location for placement. Many papers are written on the topic of PMU placement on the transmission system, but placement on the distribution system has unique constraints

[1]. The distribution system has unbalanced loads due to two-phase and single-phase branches off of the three-phase feeder. Distributed generation is also common with the growing number of solar installation and other small generation within the distribution system. An earlier study into the state estimation of the distribution grid written by Baran, et al. [2] uses a ranking method which is based on the interesting quantities criterion. The method uses a radial shaped network, which is a common configuration for distribution systems. A more modern approach to this problem is addressed by Yang and Roy [3]. This approach takes the full three phases into account, which eliminates errors due to an unbalanced three phase system. [4]-[5] present two more algorithms for finding optimum placement taking into account distributed generation along the network.

In addition to the constraints mentioned above, our PMU will only be looking at a single phase at any particular point. When the PMU is placed, the phase of the network it is on must be known, or inferred from the phase difference in order to give the phase measurement any meaning. Imbalances in the network will cause misinterpretations of the phase differences measured on separate phases. Obtaining measurements in different locations from the same phase would be best for monitoring power flow and monitoring phase. With all the measurements coming from one phase, and the other phases are ignored entire events could be missed, such as a single phase to ground fault.

Due to the lack of available location, the μPMUs will be placed in arbitrary phases of the distribution system. In the future the data from these assortment of known phases being measured will be compared to one another post-mortem to assess what information can be reliably retrieved from comparing the different phases.

IV. FUTURE EFFORTS / RESULTS

The purpose of the μPMU is to capture unusual events within the distribution system. One such captured event is shown in Fig. 4. Further investigation is necessary to find what caused this unusual event.

Once the μPMUs are placed along points on the grid, data will be gathered and used to analyze the validity of single phase measurements on distribution systems. After events are identified and categorized the data will be reviewed to find event specific patterns which could indicate in real time transformers failing, reclosers opening, or other events.

V. CONCLUSION

A device which estimates synchrophasors from the 120 V, consumer voltage level, creates a cheaper alternative to commercial PMUs. This gives an unparalleled view of the distribution system for which there are many applications. The μPMU will be set up across the University of Illinois campus collecting data on its distribution network providing such a view. Current efforts are directed at handling, processing, and interpreting the data generated by these units. Hardware limitations need to be overcome to accurately generate a synchrophasor using a National Instruments myRIO-1900.

Placement of PMUs on the distribution grid depend on many factors, some one which will be explored or validated once a network of μPMUs are distributed.

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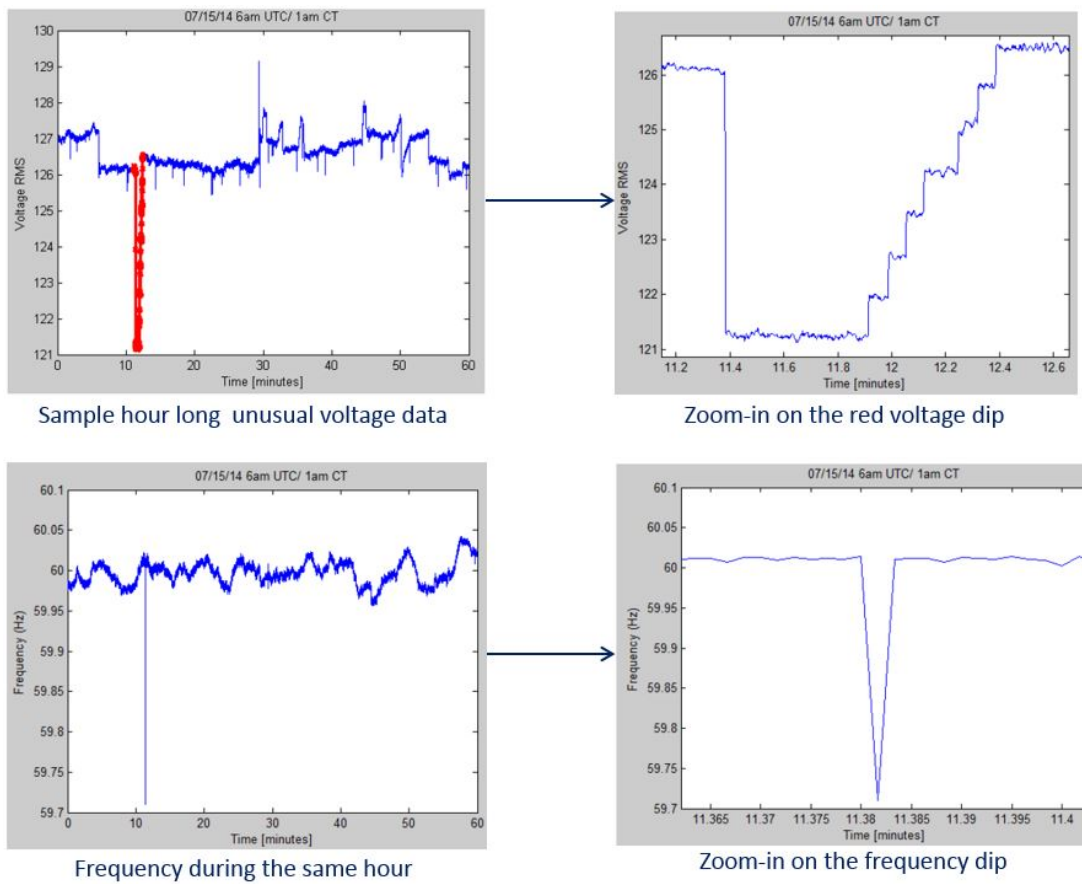
Fig. 4. Voltage dip recorded with μPMU due to an unknown event